Ferromagnetic Germanide in Ge Nanowire Transistors for Spintronics Application

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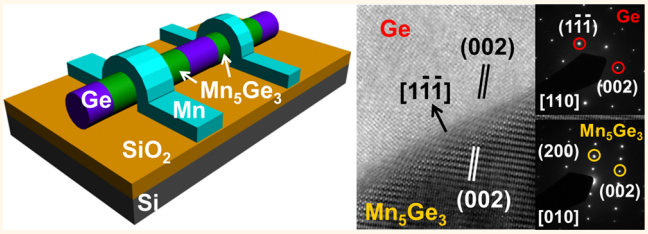
ABSTRACT



To explore spintronics applications for Ge nanowire heterostructures formed by thermal annealing, it is critical to develop a ferromagnetic germanide with high Curie temperature and take advantage of the high-quality interface between Ge and the formed ferromagnetic germanide. In this work, we report, for the first time, the formation and characterization of Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire transistors, in which the room-temperature ferromagnetic germanide was found through the solid-state reaction between a single-crystalline Ge nanowire and Mn contact pads upon thermal annealing. The atomically clean interface between Mn_5Ge_3 and Ge with a relatively small lattice mismatch of 10.6% indicates that Mn_5Ge_3 is a high-quality ferromagnetic contact to Ge. Temperature-dependent *I*—*V* measurements on the Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire heterostructure reveal a Schottky barrier height of 0.25 eV for the Mn_5Ge_3 contact to *p*-type Ge. The Ge nanowire field-effect transistors built on the Mn_5Ge_3/Ge/Mn_5Ge_3 heterostructure exhibit a high-performance *p*-type behavior with a current on/off ratio close to 10^5, and a hole mobility of 150—200 $cm^2/(V\ s)$. Temperature-dependent resistance of a fully germanided Mn_5Ge_3 nanowire shows a clear transition behavior near the Curie temperature of Mn_5Ge_3 at about 300 K. Our findings of the high-quality room-temperature ferromagnetic Mn_5Ge_3 contact represent a promising step toward electrical spin injection into Ge nanowires and thus the realization of high-efficiency spintronic devices for room-temperature applications.

KEYWORDS: germanium nanowire heterostructure · Mn_5Ge_3 · manganese germanide · atomically clean interface · spin injection

Since the discovery of the giant magnetoresistance (GMR) effect in 1980s,[1,2] numerous efforts have been made to utilize the spin of electrons as another freedom for information processing.[3−6] Among all the candidates proposed for spintronics applications, the Mn—Ge system has attracted extensive research interest as a promising material system for spintronic devices beyond scaled metal-oxide-semiconductor field-effect transistor (MOSFET).[7−14] In realizing practical spintronic devices, efficient spin injection into semiconductors and effective manipulation of spin in semiconductors are considered to be the two major challenges.[3−5] For diluted magnetic semiconductor,[7] epitaxially grown Mn-doped Ge thin films usually suffered from clusters or amorphous ferromagnetic precipitates.[15,16] Inspiringly, single-crystalline Mn-doped Ge quantum dots have been reported to exhibit electric-field controlled ferromagnetism up to 300 K.[13,14] This approach provides an effective control of the magnetic phase transition in semiconductors using a gate voltage. Meanwhile, electrical spin injection into bulk Ge using the epitaxial Fe/MgO/Ge tunnel junction has been demonstrated up to 225 K in nonlocal spin-valve measurements (although a relative low spin injection efficiency of 0.23% at T = 4 K was reported),[17] and further at room temperature with three-terminal Hanle measurements.[18,19] Moreover, lateral spin injection into Ge nanowires was also reported to manifest a spin diffusion length of more than 100 μm at low temperature,[20] and the significant enhancement in the spin diffusion length could be attributed to the effective suppression of D'yakonov—Perel' spin relaxation due to quantum confinements in the 1-dimensional (1-D) Ge nanowire channel.[21]

It is necessary to point out that the interface between the ferromagnetic metal and the semiconductor channel could play a critical role in the spin injection and detection.[22,23] This is of particular importance for Ge because of its high density of interface states, which could result in strong Fermi-level pinning close to the Ge valence band in conventional metal—Ge contacts.[24] It is also worth noting that the conductivity mismatch is another fundamental obstacle to realize efficient spin injection into

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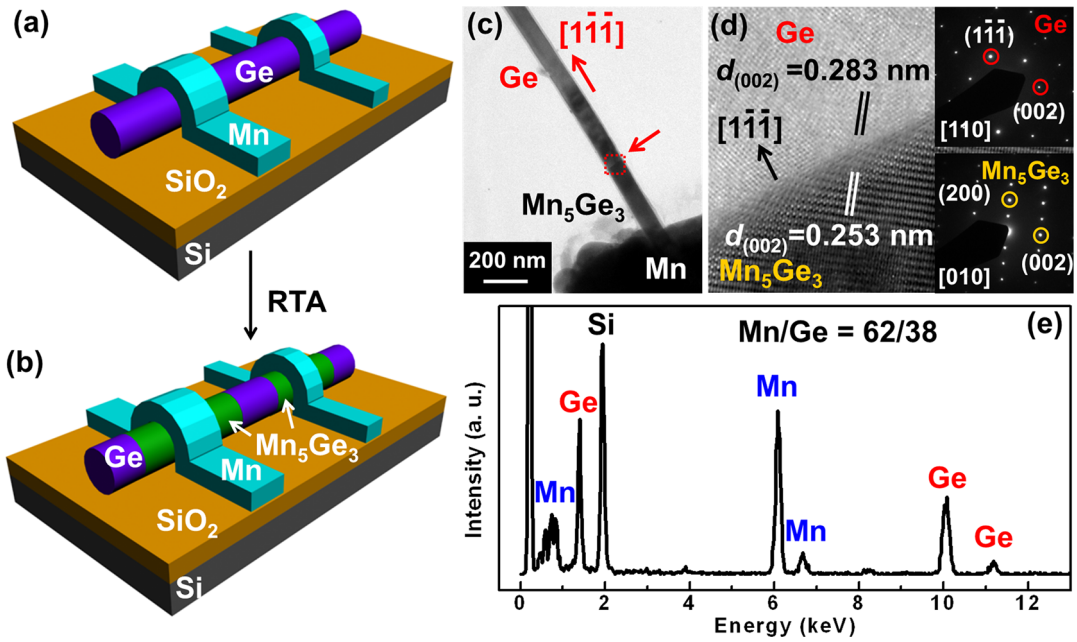

Figure 1. Formation of Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire heterostructure. Schematic illustration of (a) as-deposited Mn−Ge nanowire device structure and (b) the formation of Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire heterostructure by the solid-state reaction between a single-crystalline Ge nanowire and Mn contact pads upon rapid thermal annealing (RTA). (c) Low-magnification TEM image of a Mn_5Ge_3/Ge nanowire heterostructure. (d) High-resolution TEM image, showing an atomically clean interface between Mn_5Ge_3 and Ge with a relatively small lattice mismatch of 10.6%. The labeled lattice spacings are: d_{002} = 0.253 nm for Mn_5Ge_3 and d_{002} = 0.283 nm for Ge. The inset shows the diffraction patterns of Ge and Mn_5Ge_3. (e) EDS of the formed germanide region with a Mn/Ge atomic ratio of 62/38, confirming the phase of Mn_5Ge_3.

semiconductor due to the large conductivity difference between metal and semiconductor.[25] In solving this issue, high-quality epitaxial Fe/MgO/Ge tunnel junction grown by molecular-beam epitaxy (MBE) has been widely used in the successful demonstration of spin injection into Ge.[17,18,26] Besides the tunneling contact, Schottky contact has been theoretically shown[27] and later experimentally demonstrated in bulk Si, GaAs, and Ge[28−32] as another effective solution to overcome the conductivity mismatch problem. Again, it is crucial to maintain a high-quality interface between Ge and the ferromagnetic metal for Ge spin injection through the Schottky contact. Recently, the atomically clean interface reported in many MSi_x/Si/MSi_x and MGe_x/Ge/MGe_x (M = various metals including Ni, Pt, Co, *etc.*) nanowire heterostructures has been brought into attention for such application.[33−43] Indeed, the detection of spin-polarized carriers injected from MnSi into Si at low temperature has been reported in the MnSi/Si/MnSi nanowire heterostructure.[41] To build spintronic devices for room-temperature applications, however, ferromagnetic silicide or germanide with higher Curie temperature in such nanowire heterostructures has to be developed. In the Mn−Ge system, many manganese germanides, such as Mn_3Ge_2, Mn_5Ge_3, and $Mn_{11}Ge_8$, display ferromagnetic ordering close to or above room temperature. In particular, Mn_5Ge_3, with a Curie temperature close to 300 K, has been intensively studied as a high-efficiency spin injection source into Ge toward building Ge SpinFETs,[8−11] although most of the pioneer work has been focused on the epitaxial growth of Mn_5Ge_3 on bulk Ge. Moreover, by introducing carbon doping, the Curie temperature of $Mn_5Ge_3C_x$ can be dramatically increased up to 445 K for building practical spintronic devices that can be operated at room-temperature.[44] In this work, we report the formation and characterization of Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire transistors *via* the solid-state reaction between a single-crystalline Ge nanowire and Mn contact pads upon rapid thermal annealing (RTA). This work reports the formation of ferromagnetic germanide in Ge nanowire transistors with high-quality interfaces through thermal annealing.

RESULTS AND DISCUSSION

Figure 1 panels a and b schematically illustrate the formation process of the Mn−Ge nanowire heterostructure. Transmission electron microscopy (TEM) studies were performed in order to identify the formed germanide phase and the epitaxial relationship in the Mn−Ge nanowire heterostructure. Mn−Ge nanowire devices for TEM studies were fabricated on Ge nanowires with [111] growth directions, which were dispersed on special TEM grids with 50 nm thick Si_3N_4 windows and patterned by e-beam lithography and subsequent e-beam deposition of 150 nm thick Mn. To prevent Mn oxidization, a layer of 5 nm Ti followed by 20 nm Au was capped on Mn electrodes. The diffusion of protection metals (Ti/Au) into Ge nanowires was not observed. Other protection layers, such as Ti/Pt, Ti/Al,

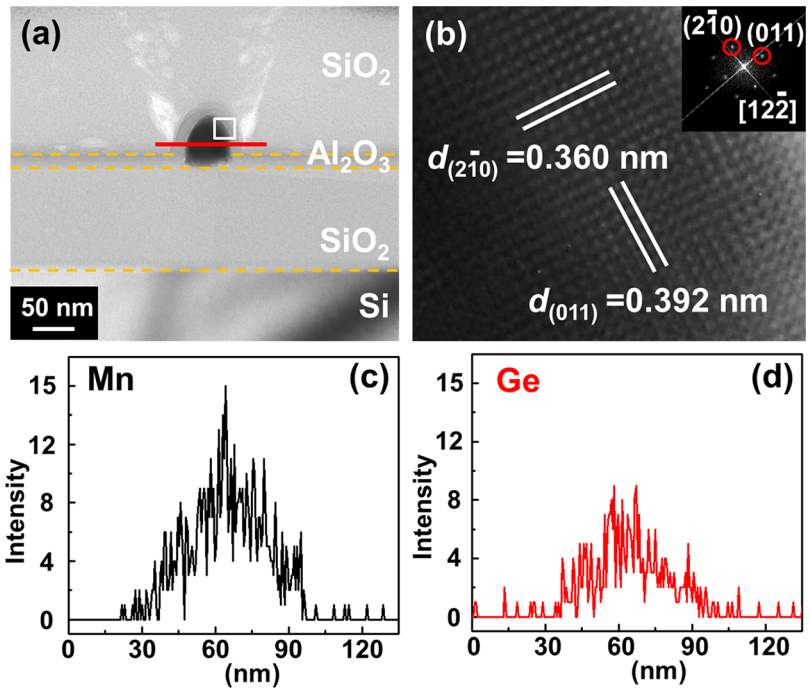

Figure 2. Cross-sectional TEM study of a Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire device. (a) TEM cross-sectional view of the formed Mn_5Ge_3 nanowire capped with 20 nm Al_2O_3 on the SiO_2/Si substrate. (b) High-resolution TEM image of the Mn_5Ge_3 region. The inset shows the corresponding diffraction pattern after fast Fourier transform. (c–d) Line-scan profiles of Mn and Ge contents in the formed germanide, respectively, reaffirming the formation of the Mn_5Ge_3 phase.

and Cr/Pt, were also tested to cap the Mn electrodes, and they all showed the same results. The samples were then loaded into the TEM chamber for *in situ* annealing to drive Mn diffusion into Ge nanowires. The formed single-crystalline germanide was identified to be Mn_5Ge_3 based on the following TEM studies. Figure 1c shows the TEM image of a typical Mn_5Ge_3/Ge nanowire heterostructure upon 450 °C RTA inside the TEM chamber. The high-resolution TEM image in Figure 1d demonstrated an atomically clean interface between Mn_5Ge_3 and Ge. Similarly, such high-quality interface has also been observed in many Ge and Si nanowire heterostructures, which is one of the unique properties in the effort of making nanoscale contacts to one-dimensional semiconductor channels through thermal annealing. The nearly constant Ge concentration in the line-scan profile of a Mn_5Ge_3/Ge nanowire heterostructure suggests that Mn is the dominant diffusion species in the Mn–Ge nanowire system (see Figure S1 in Supporting Information). The diffraction patterns in the inset of Figure 1d revealed the epitaxial relationship to be [010]Mn_5Ge_3(002)//[110]Ge(002). The formed Mn_5Ge_3 has a hexagonal structure (space group $P6_3/mcm$) with lattice constants: a_{hex} = 0.7184 nm and c_{hex} = 0.5053 nm. The lattice spacings were determined to be d_{002} = 0.253 nm for Mn_5Ge_3-(002) planes and d_{002} = 0.283 nm for Ge(002) planes, respectively. The spacing difference gives a relatively small lattice mismatch of 10.6% compared with that reported in Mn–Si nanowire and Ni–Ge nanowire systems.[39,41,42] It is suggested that the one-dimensional growth of germanide(silicide) in the Ge(Si) nanowire can accommodate substantially large lattice mismatch while maintaining an atomically sharp interface between the Ge(Si) nanowire and the formed germanide(silicide) (see Table S1 in Supporting Information). One possible explanation would be that the epitaxial growth in the Si(Ge) nanowire happens on a very small area, that is, the cross-section of the Si(Ge) nanowire, so that the energy required to form dislocations could be large. However, in the thin film epitaxy case, the epitaxial area is very large, typically over the entire substrate. Therefore, the accumulated strain is easily relaxed, which leads to the formation of noticeable defects such as threading dislocations. Further growth dynamic analysis would be necessary and also very interesting to understand the detailed mechanism. The energy-dispersive spectrum (EDS) in Figure 1e indicated a Mn/Ge atomic ratio of 62/38, which reaffirms the formed Mn_5Ge_3 phase. The Si peak was originated from the Si_3N_4 window on the TEM grid. Besides, exceeding annealing could convert a Ge nanowire into a single-crystalline Mn_5Ge_3 nanowire, and it is shown that the Mn_5Ge_3 phase was thermally stable under the annealing condition (see Figure S3 in Supporting Information).

To investigate the cross-sectional view of the formed germanide, Mn–Ge nanowire devices were fabricated on the SiO_2/Si substrate as to be described below (see Figure 3). Focused-ion beam (FIB) was used to cut the germanide region into a 50 nm thick slice as shown in Figure 2a, which was placed on a carbon-supported

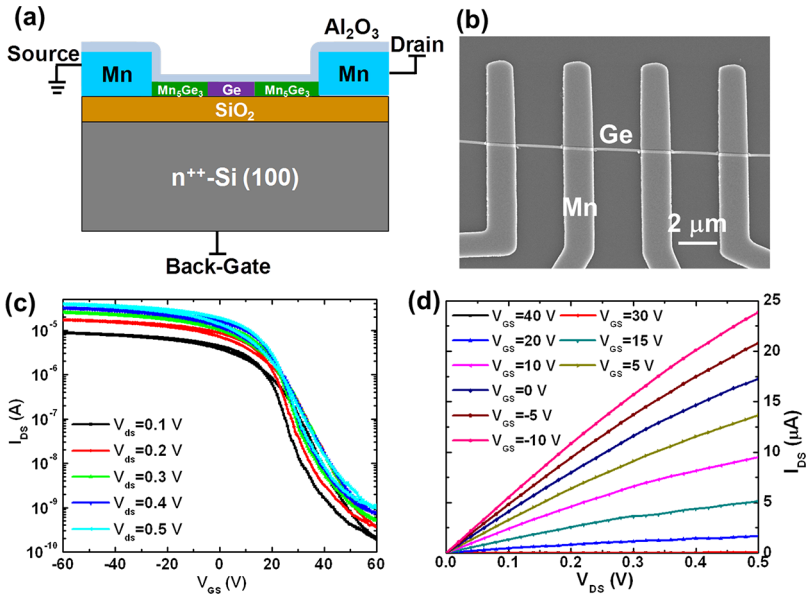

Figure 3. Characterization of a back-gate Ge nanowire FET. (a) Schematic illustration of the Ge nanowire FET built on the Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire heterostructure. (b) SEM image of the Ge nanowire FET device. (c) Dual-sweep $I_{DS}-V_{GS}$ characteristics of the back-gate Ge nanowire FET, showing a relatively small hysteresis. (d) The corresponding $I_{DS}-V_{DS}$ characteristics of the Ge nanowire transistor.

TEM Cu grid and then loaded into the TEM chamber for imaging. It is worth noting that, unlike the Ni−Ge nanowire system, no significant segregation of germanide nanoparticles on the germanide region was observed in the Mn−Ge nanowire system, and could be due to the relatively small lattice mismatch (~10.6%) between Mn_5Ge_3 and Ge. Figure 2b shows the high-resolution TEM image of the germanide region, and the diffraction pattern in the inset confirmed the single-crystalline Mn_5Ge_3 phase with a hexagonal lattice structure. The EDS line-scan profiles of Mn and Ge across the region indicated by the red line in Figure 2a are shown in Figure 2 panels c and d, respectively. The Mn/Ge atomic ratio is consistent with the Mn_5Ge_3 phase as well as the EDS result in Figure 1e.

Similar to Ni_2Ge and NiGe in Ni−Ge nanowire heterostructures,[39,42] the formed Mn_5Ge_3 can be used as source/drain contacts to the Ge channel for the fabrication of high-performance Ge nanowire FETs (see Figure 3a). The Ge nanowire channel length can be scaled down to sub-30 nm by controlling the annealing temperature and time (see Figure S2 in Supporting Information).[43] Mn−Ge nanowire devices for electrical measurements were fabricated on a prepatterned SiO_2/Si substrate, and Mn/Ti/Au contacts to Ge nanowires were defined with e-beam lithography followed by e-beam evaporation of the contact layers. Prior to the RTA process in the ambient of N_2, a layer of 20 nm Al_2O_3 was deposited on top with atomic layer deposition (ALD) to protect the Mn electrode and the formed germanide from oxidization. TEM studies showed that the Al_2O_3 capping layer did not affect the formed germanide phase and the growth of Mn_5Ge_3 in the Ge nanowire (see Figure 2). Figure 3b shows the scanning electron microscope (SEM) image of as-fabricated Mn−Ge nanowire devices with multiple electrodes, and the measurement setup is illustrated in Figure 3a. The $I_{DS}-V_{GS}$ characteristics of a typical Ge nanowire FET with an effective channel length of 0.5 μm after RTA and a nanowire diameter of 70 nm demonstrated a *p*-type transistor behavior with a current on/off ratio close to 10^5, as shown in Figure 3c. The dual-sweep $I_{DS}-V_{GS}$ curves showed a relatively small hysteresis, which could be attributed to the effective passivation of the Ge nanowire surface by Al_2O_3.[42] The normalized transconductance (g_m) at a drain bias of V_{DS} = 0.1 V was extracted to be 3.56 μS/μm, which led to a field-effect hole mobility of 170 $cm^2/(V\,s)$ using the equation[39,42]

$$\mu = \frac{g_m L^2}{V_{ds} C_{ox}} \quad (1)$$

Mobility measured from more than 20 devices fell into the range of 150−200 $cm^2/(V\,s)$. The gate capacitance C_{ox} here is estimated using the cylinder-on-plate model:[45]

$$C_{ox} = \frac{2\pi\varepsilon_{ox}\varepsilon_0 L}{\cosh^{-1}\left(\frac{r+t_{ox}}{r}\right)} \quad (2)$$

in which ε_{ox} = 8.85 × 10^{-14} F/cm is the vacuum dielectric constant, ε_{ox} = 3.9 is the relative dielectric constant for SiO_2, r = 35 nm is the radius of the Ge nanowire, t_{ox} = 300 nm is the thickness of the back-gate dielectric, L = 0.5 μm is the effective Ge nanowire channel length. To provide a more accurate estimation of the gate capacitance, a finite element simulation was performed by Wunnicke, which gave rise to an

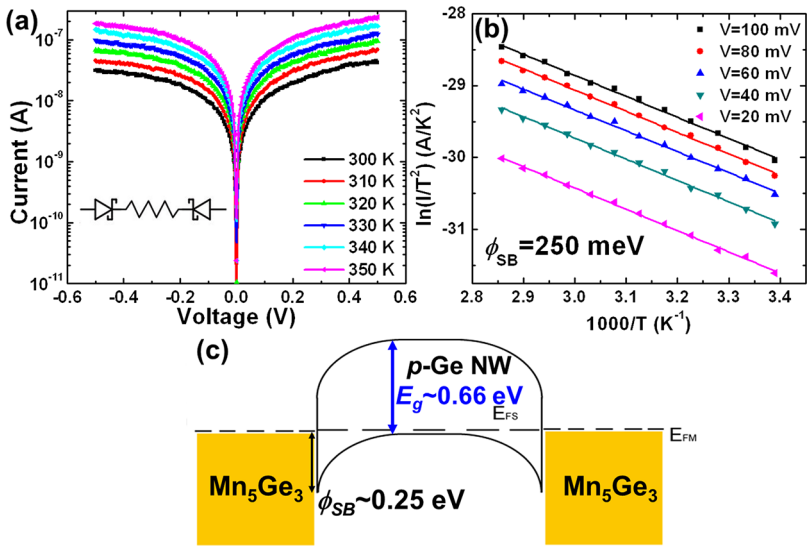

Figure 4. Temperature-dependent $I-V$ measurements on the $Mn_5Ge_3/Ge/Mn_5Ge_3$ nanowire heterostructure. (a) $I-V$ measurements on a $Mn_5Ge_3/Ge/Mn_5Ge_3$ nanowire heterostructure in the temperature range of 300−350 K. (b) Arrehenius plot at various drain biases. The extracted Schottky barrier height from Mn_5Ge_3 to p-type Ge is about 0.25 eV. (c) Corresponding energy band diagram of the $Mn_5Ge_3/Ge/Mn_5Ge_3$ nanowire heterostructure.

effective dielectric constant of $\varepsilon_{ox,eff}$ = 2.2 for SiO_2 in eq 2.[45] Then the calculated gate capacitance and mobility would be $C_{ox} = 2.074 \times 10^{-17}$ F and μ_h = 301 $cm^2/(V\,s)$, respectively. Therefore, the value of μ_h = 170 $cm^2/(V\,s)$ using ε_{ox} =3.9 for SiO_2 is the lower limit for the carrier mobility estimation. The subthreshold swing was also extracted to be about 3.81 V/dec for a relative thick back-gate dielectric of 300 nm SiO_2. The $I_{DS}-V_{DS}$ characteristics in Figure 3d reaffirmed that Mn_5Ge_3 are good source/drain contacts.

To further evaluate the Mn_5Ge_3 contact to Ge, temperature-dependent $I-V$ measurements were performed on a $Mn_5Ge_3/Ge/Mn_5Ge_3$ nanowire heterostructure in the temperature range of 300−350 K, and the results are shown in Figure 4a. Figure 4b shows the linear fitting of $\ln(I/T^2)$ versus $1/T$ in the Arrehenius plot at various drain biases revealing a consistent Schottky barrier height of 0.25 eV. The corresponding band diagram for the $Mn_5Ge_3/Ge/Mn_5Ge_3$ nanowire heterostructure is drawn in Figure 4c. Recalling the above-mentioned high-quality epitaxial interface of Mn_5Ge_3 on Ge and the room-temperature ferromagnetism of Mn_5Ge_3, it is promising to realize spin injection from Mn_5Ge_3 into Ge nanowires through this Schottky barrier. It is worth mentioning that heavily doped Ge nanowires are usually required to overcome the fundamental obstacle of the conductivity mismatch between metallic Mn_5Ge_3 and semiconducting Ge.[25] Indeed, both theoretical calculations and experimental work have been carried out to investigate Mn_5Ge_3 as a high-efficiency spin injection source into Ge.[8−11] Most of the pioneer experimental work has been focused on the epitaxial growth of Mn_5Ge_3 on bulk Ge, and the Mn_5Ge_3 epilayer on both Ge (111) and GaAs (111) substrates was reported to have a spin polarization of about 42% at T = 1.2 K from Andreev reflection measurements.[10] However, the 1-D Mn−Ge system may offer great advantages in spintronics applications since the D'yakonov−Perel' spin relaxation could be significantly suppressed in the 1-D regime.[21] Therefore, a long spin diffusion length could be expected in the $Mn_5Ge_3/Ge/Mn_5Ge_3$ nanowire heterostructures. Furthermore, to observe the spin signal at room temperature and above, carbon doping can be incorporated into Mn_5Ge_3 to dramatically boost the Curie temperature: $Mn_5Ge_3C_x$ films with carbon concentration $x \geqslant 0.5$ showed a Curie temperature up to 445 K while maintaining the hexagonal lattice structure.[44] Finally, the Ge nanowire can be fully germanided by carefully controlling the annealing time.

The magnetic property of a fully germanided Mn_5Ge_3 nanowire was also studied. Figure 5a shows both two-probe and four-probe $I-V$ measurements on a 650 nm-long single-crystalline Mn_5Ge_3 nanowire in order to exclude the contact resistance. The inset shows a typical SEM image of a fully germanided Mn_5Ge_3 nanowire with four electrodes. Figure 5b shows the temperature-dependent resistance and resistivity of the Mn_5Ge_3 nanowire using a standard four-probe measurement technique. The resistivity of the formed single-crystalline Mn_5Ge_3 nanowire was extracted to be 240 $\mu\Omega$-cm at 300 K, and slightly saturated at about 46.5 $\mu\Omega$-cm at temperatures below 10 K. The monotonic decrease in the resistance with respect to the temperature affirms the metallic behavior of Mn_5Ge_3. The resistivity change ratio, $\rho(300\text{ K})/\rho(2\text{ K}) \approx 5.2$, is much larger than that for a normal metal due to the spin-dependent magnetic scattering in ferromagnetic Mn_5Ge_3. More importantly, a clear transition in the $R-T$ curve was indicated by the arrow, and the transition temperature is related to the magnetic phase

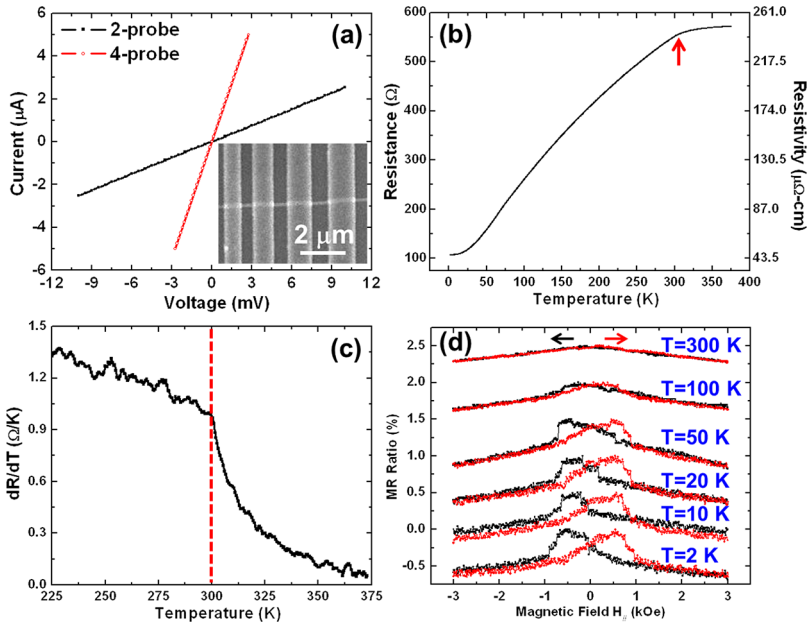

Figure 5. Electrical transport study of the formed single-crystalline Mn_5Ge_3 nanowire. (a) 2-probe and 4-probe *I*−*V* measurements on a fully germanide Mn_5Ge_3 nanowire at 300 K. The inset shows the SEM image of a typical fully germanided Mn_5Ge_3 nanowire with four electrodes. (b) Temperature-dependent resistance and resistivity of a Mn_5Ge_3 nanowire using a standard 4-probe measurement technique. The extracted resistivity at 300 and 2 K is about 240 $\mu\Omega$-cm and 46.5 $\mu\Omega$-cm, respectively. The arrow indicates the transition temperature, which is close to the Curie temperature of Mn_5Ge_3 (about 300 K). (c) The differential of the resistance with respect to the temperature, manifesting the transition temperature close to 300 K. (d) MR ratio of the Mn_5Ge_3 nanowire at different temperatures from $T = 2$ K up to 300 K. The MR data show ferromagnetic hysteretic behaviors of the Mn_5Ge_3 nanowire during the in-plane magnetic field sweeping. MR curves at different temperatures are intentionally offset by multiples of 0.5%. The black and red arrows indicate the corresponding magnetic field sweeping direction.

transition temperature of Mn_5Ge_3, i.e., the Curie temperature of about 300 K.[10,41] Figure 5c shows the differential of resistance with respect to temperature, which further manifests the transition temperature around 300 K. Figure 5d shows the MR ratio of the Mn_5Ge_3 nanowire at different temperatures from $T = 2$ K up to 300 K. Here the MR ratio is defined by $MR = [(R_H - R_{max})/R_{max}] \times 100\%$, and MR curves at different temperatures are intentionally offset by multiples of 0.5%. The hysteretic behaviors during the in-plane magnetic field sweeping further affirm the ferromagnetic property of the Mn_5Ge_3 nanowire.

CONCLUSIONS

In summary, a Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire heterostructure with atomically clean interfaces has been formed by the thermal intrusion of Mn into a single-crystalline Ge nanowire at 450 °C. TEM studies revealed an epitaxial relationship of [010]Mn_5Ge_3(002)//[110]Ge(002) with a relatively small lattice mismatch of 10.6% between Mn_5Ge_3(002) and Ge(002) planes. Back-gate Ge nanowire FETs have been fabricated on the Mn_5Ge_3/Ge/Mn_5Ge_3 heterostructure by using the formed Mn_5Ge_3 region as the source/drain contacts to the Ge nanowire channel. Electrical measurements have shown a high-performance *p*-type transistor behavior with a current on/off ratio close to 10^5, and a field-effect hole mobility of 150−200 $cm^2/(V\ s)$. The Schottky barrier height from the Mn_5Ge_3 contact to *p*-type Ge extracted from the temperature-dependent *I*−*V* measurement was about 0.25 eV; the result suggested that Mn_5Ge_3 may be used as a promising spin injection source into Ge nanowires. Moreover, the temperature-dependent resistance of a fully germanided Mn_5Ge_3 nanowire demonstrated a metallic behavior with a clear transition near the Curie temperature of Mn_5Ge_3 at about 300 K. This work represents a promising step toward electrical spin injection into Ge nanowires and thus realization of high-efficiency spintronic devices. Our findings of the high-quality epitaxial interface and room-temperature ferromagnetic germanide in the Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire heterostructure, together with the prior demonstrated gate control of paramagnetism to ferromagnetism transition in diluted magnetic Ge,[13] will serve as the foundation to build room-temperature Ge SpinFETs.

EXPERIMENTAL METHODS

Single-crystalline Ge nanowires with growth direction along [111] axes were synthesized vertically on a Si (100) wafer using a conventional vapor−liquid−solid (VLS) method as described elsewhere.[46] To control the nanowire diameter and length, dodecanethiol-coated Au nanoparticles were prepared by self-assembly on a Si (100) substrate to serve as the catalyst for the Ge nanowire growth. The precursor diphenylgermane was injected into the reactor to stimulate the nanowire growth at 420 °C.[47] The VLS-grown Ge nanowires were typically

50−80 nm in diameter with lengths larger than 10 μm. Ge nanowires were not doped on purpose during growth, but unintentional doping usually occurred.[48,49]

To prepare TEM samples, VLS-grown Ge nanowires were dispersed on TEM grids whose Si_3N_4 windows were fabricated by etching bulk Si out of Si_3N_4/Si, and the 50 nm thick low-stress Si_3N_4 film was deposited by low-pressure chemical vapor deposition (LPCVD). Mn/Ti/Au contacts (150/5/20 nm thick) to the Ge nanowire were defined with e-beam lithography followed by subsequent e-beam evaporation. Before the metal deposition, the sample was dipped into diluted hydrofluoric acid (HF) for 15 s to completely remove native oxide in the contact region. The as-fabricated Mn−Ge nanowire devices were then loaded into the TEM chamber with a heating holder (Gatan 652 double tilt heating holder) for *in situ* annealing under a RTA mode with a pressure below 10^{-6} Torr. The temperature was ramped from room temperature up to 450 °C at a rate of about 25 °C/s. A field-emission TEM (JEM-3000F, operated at 300 kV with a point-to-point resolution of 0.17 nm) equipped with an energy-dispersive spectrometer was used to obtain the epitaxial relationships and determine the chemical compositions of the nanowire heterostructure.

To fabricate Mn−Ge nanowire devices for electrical measurements, VLS-grown Ge nanowires were transferred onto a pre-patterned SiO_2/Si substrate. The top thermal SiO_2 was 300 nm thick, and the Si substrate was degenerately doped to have a resistivity of $1-5 \times 10^{-3}$ Ω-cm, which served as the back-gate for further device characterization. E-beam lithography was used to define Mn/Ti/Au contacts to Ge nanowires followed by the e-beam evaporation. Before the metal deposition, the sample was dipped into diluted HF solution for 15 s to completely remove native oxide in the contact region similar to before. Prior to the RTA process in the N_2 ambient, the Mn−Ge nanowire device was capped with 20 nm Al_2O_3 using ALD. The morphology of Mn−Ge nanowire devices was inspected using a field-emission SEM. Electrical measurements were performed using a homemade probe station connected to a Keithley 4200 semiconductor parameter analyzer. Temperature-dependent measurements and magnetotransport studies were performed with a Quantum Design physical property measurement system (PPMS).

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Line-scan profile of a Mn_5Ge_3/Ge nanowire heterostructure; literature review of the lattice mismatch in Si and Ge nanowire heterostructures; TEM images of a Mn_5Ge_3/Ge/Mn_5Ge_3 nanowire device with sub-30 nm Ge channel; TEM image of a fully germanided Mn_5Ge_3 nanowire after exceeding annealing; lattice sketch of the Mn_5Ge_3/Ge interface. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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